

DATA ACQUISITION SUBSYSTEM

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ABSTRACT- A data acquisition system is described. The system connects to a DEC VAX 750 computer and allows it to perform A/D and D/A operations at rates up to 100kHz. It also can perform multichannel low speed operations for physiological channels. It allows for raster graphic and vector graphic displays. The system is partially complete and currently in use at the Speech, Hearing and Language Research Centre at Macquarie University.

INTRODUCTION

The Speech, Hearing, and Language Research Centre (SHLRC) at Macquarie University has developed a peripheral for the Digital Equipment Corporation (DEC) VAX computer which allows it to perform precision real time analog Input and Output (I/O). The peripheral is a single card which acts as a programmable First In First Out (FIFO) buffer. This FIFO is attached to the standard VAX Direct Memory Access (DMA) card, the DR11W. Up to 8 FIFOs can be connected to each DMA card.

The FIFO is an intelligent buffer which is dynamically programmable. The standard VAX/VMS operating system calls are used to control the FIFO. The FIFO can be Reset, configured, and data can be sent and received by using the VMS SYS\$QIO call. The FIFO can be programmed to be an input or output buffer, and the buffer can have it's size changed. The FIFO can be programmed to clock data out of the buffer into a D/A, or to clock data in from an A/D, or to control other slaves.

The FIFO is currently being used by the SHLRC on it's VAX 750 computer as an analog data acquisition system. The implementation currently uses 1 FIFO, but 3 are planned, using attached A/Ds and D/As. The FIFO is set up as a high speed channel, used for the Left channel of an audio system. It has a companion 16 bit A/D and D/A converter capable of sampling at up to a 100kHz rate. The second FIFO will be set up the same as the first and will be used for the Right channel of the audio system. The third FIFO will be set up as 16 low speed channels, used for physiological data gathering. It will have a companion 12 bit A/D and D/A converter sampling at up to a 1kHz rate with a 16 channel multiplexer. There are 5 spare slots for further applications.

VAX SOFTWARE

The VAX software to control the FIFO, is straight forward and uses no special routines or drivers. The SYS\$QIO and SYS\$QIOW system calls are used from FORTRAN to send and receive data to and from the FIFO via the VAX DMA unit. The SHLRC VAX 750 currently uses VMS Version 4.1 and to date, no bugs have been found. There was a bug in VMS Version 3.5 which caused the whole VAX to crash under certain conditions.

There are currently 4 different projects and programmers using the FIFO. One project is developing a speech editor which is using it for speech output. Another project is developing a Text To Speech (TTS) system in conjunction with a digital speech synthesiser, and using it for synthesiser output. Another is developing a hearing test for air traffic controllers and using it for speech output. Another is using a software vocoder pair to investigate frequency and time resolution of speech signals and it is also using it for speech output.

The program using the FIFO must first assign and allocate the DMA unit. Then the FIFO must be reset to put it into a known state. A block of 4 words is then sent to the FIFO to configure it. Then the actual data is transferred.

The first word in the configuration block is the mode that the FIFO is required to operate in. The possible modes are:

- 0 = High Speed A/D (input)
- 1 = High Speed D/A (output)
- 2 = Low Speed A/D (input)
- 3 = Low Speed D/A (output)
- 4 = Echo (input to (output)
- 5 = Centronix (output)
- 6 = Raster graphics (output)
- 7 = Vector graphics (output)

The next word in the configuration block is the transfer block size. The data is transferred between the VAX and the FIFO in blocks. They can be programmed to be any size from 1 word to 4000 words.

The next word is the sampling rate. This is used to program the 80186 timer to provide clocked data transfers to and from the slave. The rate can be any frequency between 30Hz and 2MHz.

The last word in the configuration block is the number of channels to be scanned. This will be 1 for the High speed channels, but it can be from 1 to 16 for the Low speed channels.

Now that the FIFO has been configured, the data transfer can begin. The same calls are used for all FIFO communication.

FIFO STRUCTURE

The FIFO can be functionally divided into 3 sections: the VAX interface, the processor, and the slave interface.

VAX INTERFACE

This section contains the signal conditioning and DMA transfer control logic. The VAX interface contains bus transceivers and signal conditioning components for the signals between the FIFO and the VAX. These signals control the data flow, convey the status of the FIFO and the VAX and carry the data between them.

The FIFO can be interrupted, reset, and reconfigured, at any time by the VAX.

The VAX transfers a 16 bit word on the data lines to the interface, where it is latched, and a flag is set. The FIFO then takes the data and requests more from the VAX. The interface contains flags to show the VAX and the FIFO the status of the transaction. The reverse direction (the FIFO to the VAX) functions in an identical manner.

The VAX has 3 lines which the interface interprets as address lines. Using this, the VAX DMA unit can select up to 8 different FIFO's on the one DMA unit. The FIFO echoes this address so that the VAX can determine how many FIFO's are on line.

The other signals are used to control the direction of data flow, to show the VAX ready status, the VAX busy signal, and a request line which the FIFO uses to ask for a data transfer.

There are 2 Light Emitting Diodes (LED) which show the condition of the FIFO. When the FIFO is reset, the red LED is off and the green LED is flashing to indicate that the FIFO has completed self checks and is ready for configuring. When the FIFO has been configured, the green LED ceases flashing and stays on. The red LED represents the "OUT OF DATA" condition and lights when the FIFO has exhausted it's data and requires more. During data transfers the red LED will be off and the green LED will be on.

CONTROL PROCESSOR

This section contains the controlling microprocessor. It contains 2 buffers in on board Random Access Memory (RAM) of programmable size which constitutes the actual FIFO. The FIFO processor is the INTEL iAPX80186 16 bit microprocessor, which manages both interfaces. It has 16 kilobytes of RAM and 8 kilobytes of Read Only Memory (ROM). The ROM contains the control program for the FIFO and the RAM is the buffer. The 80186 has 2 onchip DMA units. One is used to transfer the data between the VAX and one buffer, and the other is used to transfer the data between the other buffer and the slave. When one of the buffers is emptied, they are swapped and then refilled. The 80186 has an onchip timer, and this is used for clocked data transfers when required. The 80186 also has an onchip Priority Interrupt Controller which is used to schedule the DMA interrupts at buffer changeover time. The 80186 also has onchip programmable device select lines. This eliminates any device select logic and simplifies the hardware design. The 80186 address lines and data lines are buffered before they connect to the ROM, the RAM, the VAX interface, and the slave interface.

SLAVE INTERFACE

This section is an interface to the slaves, and contains the signal conditioning logic. The slave interface has 2 different physical ports. One is the S100 bus itself. The FIFO can become bus master and can read and write to any I/O devices on the S100 bus. The other physical port is a connector on the top of the FIFO card, and this is arranged in a similar manner to a centronix printer. The data transfer protocol on both ports can operate in 4 different ways.

1/ The 80186 timer can clock the data transfers between the slave and the FIFO, at any rate between 30Hz and 2MHz. The rate is programmed at configuration time.

2/ The data can be clocked between the slave and the FIFO at the rate of an external clock. This allows 2 FIFOs to be synchronised together.

3/ The data transfer can be controlled by the slave. This allows the slave to control the speed of the transfer, as the slave indicates when it requires a data transfer, and the FIFO responds.

4/ The data transfer can be done by polling the slave. The FIFO processor will repeatedly poll the S100 bus, and read the status of an S100 slave. When the status is correct the transfer of the data can take place.

FIFO STATUS

The FIFO design is still in flux, as not all the functions and not all its combinations have been tested. To date, the FIFO has been tested for analog output at 150KHz sample rates (clocked output), driving a printer at 180cps (centronix output), and synthesiser output (slave demanded rates). The high speed analog input and raster graphics channels are currently under development.

There are 2 high speed analog channels, 1 low speed analog channel, 1 synthesiser channel, 1 raster graphic channel, and 1 vector graphic channel planned for the final implementation. Thus there will be 2 as yet unallocated channels left (out of the possible 8) before a second VAX DMA unit is required.

FIFO SOFTWARE

The FIFO software is written in 80186 assembler language and is still under development. The software after reset, initialises all the flags, all the pointers, sets up the programmable memory map, and then does a self check. The VAX and the slave ports are reset and the Priority Interrupt Controller is configured. The DMA units are programmed when required after the mode has been determined.

The green LED is, at this point, flashed while the 80186 waits for the configuration parameters from the VAX. When the parameters have been obtained the green LED is turned on and left on to indicate the reception of them.

The parameters are now analysed. The timer is set to the correct clock speed. The mode is checked and the correct routine is entered. There is a separate routine for each mode.

Each mode then configures the DMA units as to the direction of transfer and the block size, and the DMA is armed. The DMA will now wait for the data. At the end of each data transfer (i.e. when a block has been sent) an interrupt causes the processor to swap the buffers and then begin to fill the one just emptied. The red LED will light when it cannot fill the empty one.

Only modes 1, 4, and 5 have been currently tested. The other modes are still under development.

I/O CHANNELS

Each I/O channel consists of a FIFO and a companion card. The high speed channel uses 1 FIFO and 1 analog card. There will be 2 high speed channels, one for the Left channel and one for the Right channel of an audio system. They both use the top slave port on the FIFO. The low speed channel consists of 1 FIFO and a companion analog card. There will be 1 low speed channel, and this will have 16 analog inputs and 16 analog outputs. This also uses the top slave port on the FIFO.

Using this arrangement allows the 6 cards (3 FIFOs, 2 high speed, 1 low speed analog card) to be on the same S100 bus backplane and card frame. The slave ports used are on the top of the FIFOs and are joined by ribbon cables between pairs of cards (1 FIFO to 1 slave), and they only use the bus as a power supply. The S100 bus is free for a polled slave. The present raster graphics system is a polled arrangement. This consists of 5 S100 bus cards (4 bit planes and 1 palette) which will be the companion for 1 FIFO.

HIGH SPEED ANALOG CHANNEL

The high speed Left and Right audio channel companion cards each have a 16 bit D/A converter and a 16 bit A/D converter. These are the BURR BROWN type PCM53JGV and PCM75KG. They are both capable of sampling at 100kHz. At this time the D/A has been tested OK at a sample rate of 150kHz for 1 channel only. This high speed analog card connects to the top slave port on the FIFO. The A/D section and multiple channel combinations have not been tested yet. The analog card also has a switched capacitor antialiasing filter for the A/D and an identical one for the D/A. The question of the final type of filters and the programmability of them has not been finalised yet. The audio input and output lines to the card are 600 ohm balanced.

LOW SPEED CHANNEL

There will be one low speed analog channel which will consist of 1 FIFO and 1 analog card. They will communicate through the top slave port on the FIFO. The analog card will contain a 12 bit A/D with a 16 position multiplexer. This will allow 16 analog inputs to be selected. A standard 16 input 12 bit A/D module will be used. Typical inputs will be low frequency physiological signals from air flow and muscle transducers. The output will be similar, with sixteen 12 bit D/A analog outputs for non specific purposes. The data will be transferred as a 16 bit word for each input (or output). It will be arranged as 12 bits of actual sample and 4 bits of address which denotes the input selected. The sample rate will be selectable up to 1kHz.

RASTER GRAPHICS CHANNEL

The raster graphics channels will consist of 1 FIFO and 5 graphics cards. The graphics cards have been transferred over from the SHLRC's old minicomputer. They will work with polled slave transfers using the S100 bus. The raster graphics set consists of 4 Microangelo bit planes which each produce a 512x512 pixels resolution with built in graphics primitives. Each card has an on board graphics processor. The other card is a Palette which combines the the 4 bit planes and interprets this as a Z axis value of 16 possible intensity levels. Thus the total resolution becomes 512x512x16. The 16 values for each of the 512x512 pixels, use the palette lookup table which can be programmed to provide any 16 colours out of a possible 16.8 million colours. These can be 16 grey levels, if required, which is suitable for a computer generated spectrogram.

SYNTHESISER CHANNEL

A speech synthesiser is presently connected to a FIFO on the VAX. It uses the top slave port. Since the synthesiser mimics a centronix printer, it connects directly. The data from the TTS program in the VAX sends the speech parameters through the FIFO to the synthesiser which then speaks. The system is currently undergoing further testing, both to refine the TTS package and to accelerate the parameter transfer.

PLANNED I/O DEVICES

A vector graphic system is undergoing design which uses 1 FIFO and a companion D/A card. The connection to the FIFO will be on the the top slave port, and so will not use the S100 bus. This will provide an XY display of 1024x1024 resolution. The D/A card has two 10 bit D/A blocks for the XY directions. The vector graphic display has been proved in use, to be superior to raster graphics for quick waveform display. It will be continuously refreshed by the FIFO and has a refresh rate faster than the SHLRC's present vector display, which flashes when a large amount of pixels (about 1000) are displayed. The new system will show up to 4000 pixels without flashing.

CONCLUDING REMARKS

The data acquisition system shows great promise and to date has exceeded the design criteria. It has already proved versatile enough to be applied in ways not originally envisaged. Development is continuing.

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